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5 GHz CASCADED CMOS LNA WITH POSITIVE FEEDBACK FOR LOW POWER APPLICATION

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KEYWORDS: CMOS, low-noise amplifier (LNA), positive feedback, ultra-low power, ultra-low voltage.

ABSTRACT
A novel circuit topology for a CMOS low-noise amplifier (LNA) is presented in this paper. By employing a positive feedback technique at the common-source transistor of the cascade stage, the voltage gain can be enhanced.

In addition, with the MOS transistors biased in the moderate inversion region, the proposed LNA circuit is well suited to operate at reduced power consumption and supply voltage conditions. Utilizing a standard CMOS process, the CMOS LNA has been demonstrated for 5-GHz frequency band applications. Operated at a supply voltage of 0.6 V, the LNA with the gain-boosting technique achieves a gain of 17 dB and a noise figure of 2.1dB. This CMOS LNA will be planned to work for military applications.

INTRODUCTION
Low noise amplifier is used to amplify the incoming weak signals without affecting them by noise, and to improve the signal parameters. The low noise amplifier is placed at the radio receiver RF front end. Receiver receives the radio waves and converts their information to a suitable form. It consists of major blocks as switch, band pass filter, low noise amplifier, mixer. The information carried by the radio waves is affected by the noise. Noise which acts as an unwanted signal degrades the quality of information. So the noise parameter is of prime importance [1]. The low noise amplifier needs to have low noise figure, high gain and good stability to avoid oscillations.

In the present technology the transistors are used for amplification purpose. All the signal parameters are improved due to the use of transistors. In this design of low noise amplifier low noise figure, high gain, good stability and input output matching all these parameters should work together hand in hand [2].

To overcome the stringent limitations imposed by ultra-low supply voltage and ultra-low power dissipation, a cascade LNA topology is presented in this paper. By operating the transistors in moderate inversion, the LNA circuit can operate at microwatt power consumption. By incorporating a positive feedback technique in the proposed topology, enhanced gain can be achieved at the frequency band of interest. The aspect ratio and gate bias of M3 are optimized for optimum voltage gain, noise figure, linearity, and stability for the proposed LNA. Using a standard 0.13-µm CMOS process, the proposed CMOS LNA is implemented for the 5-GHz band applications.

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DESIGNED BLOCK DIAGRAM

The designed two stage cascaded CMOS LNA is designed by using the following blocks.

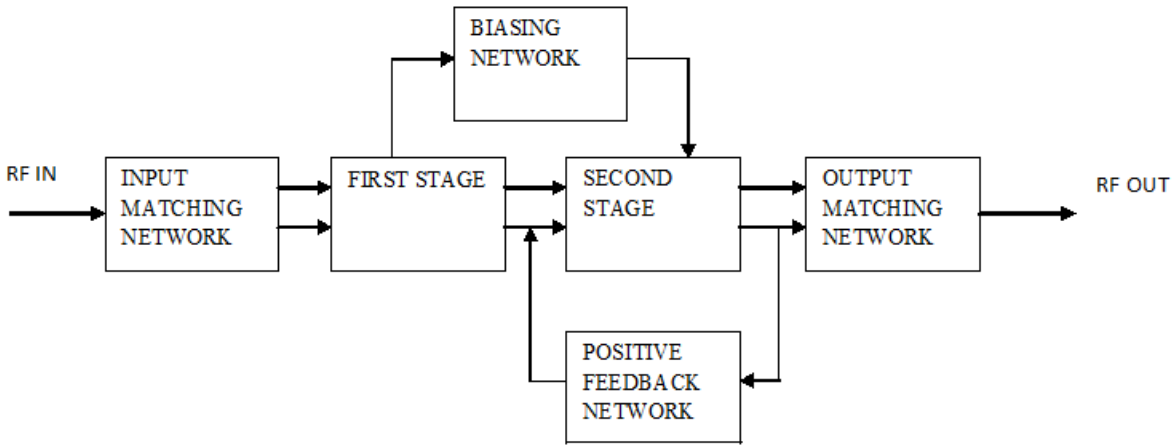

Figure 1. Block Diagram

Since the LNA is the first component in the receiver chain, the input must be matched to be driven by 50Ω. Many methods for matching the input using passive circuit elements are possible with varying bandwidths and degrees of complexity.

Impedance matching is the practice of designing the input impedance of an electrical load or designing the output impedance of its corresponding signal source to maximize the power transfer or to minimize signal reflection from the load. In the case of a complex source impedance Z_S and load impedance Z_L, maximum power transfer is obtained when Zs = Zl*, where Z_S represents the characteristic impedance of a transmission line, minimum reflection is obtained when Zs = Zl.

Impedance matching to minimize reflections is achieved by making the load impedance equal to the source impedance. If the source impedance, load impedance and transmission line characteristic impedance are purely resistive, then reflection-less matching is the same as maximum power transfer matching. If the source has a reactive component, but the load is purely resistive then matching can be achieved by adding a reactance of the opposite sign to the load. This simple matching network consisting of a single element will usually only achieve a perfect match at a single

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frequency. This is because the added element will either be a capacitor or an inductor, both of which are frequency dependent and will not follow the frequency dependence of the source impedance.

Combinations of transformers, resistors, inductors, capacitors and transmission lines are used to match electrical impedances.

Designed LNA requires an inductor to provide the power and noise match. It is simple and in series with the input of the transistor. It achieves simultaneous noise and power matching of the transistor.

For CMOS circuit implementations, the most widely used circuit schematic is a common-source amplifier with source degeneration for ultra-low-supply voltage. In order to effectively enhance the voltage gain at ultra-low-supply voltage, positive feedback can be incorporated in the common-source amplifier with source degeneration. Based on a simple concept, it can be accomplished by inserting a Tran's conductance stage. With the designed technique, the voltage gain of the source-degenerated common-source amplifier can be determined by the second stage.

The second stage of the designed LNA with a positive feedback, where current source and inductor are the Norton's equivalent circuit of the first stage. For better understanding of the gain-enhancement technique, the loop gain of the positive feedback is derived.

Here, fixed biasing technique is used everywhere to bias the transistors M1, M2, M3. The DC voltage depends on the transistor's voltage requirement being used for the amplifier design.

By employing a positive feedback technique at the common-source transistor of the cascade stage, the voltage gain can be enhanced.

CIRCUIT IMPLEMENTATION

The circuit simulation is done in the ADS (Advance Design System) software by the Agilent Company. The design using the lumped components and the TSMC RF CMOS components is done.

First Stage of Amplifier:

RF input is applied to the first stage of an amplifier. This stage will accept only the signals within selected band. In this design, the selected frequency is 5 GHz. For the design of the single stage low noise amplifier, the NMOS transistor is used. LNA designing has various topologies such as common source, common gate, and cascode topology. Here in the implemented design, first stage of LNA is a common-source amplifier with source degeneration technique. This first stage of LNA is designed mainly to dominate the noise figure of the amplifier. Biasing voltage for the amplifier is 0.55V and current is 834 µA. The input impedance and output impedance matching to the amplifier circuit is provided through the inductor.

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Second Stage of Amplifier:
For the design of the second stage of low noise amplifier, the NMOS transistor in common-source topology with source degeneration technique is used, same as in the first stage. This second stage of LNA is designed mainly to achieve the high gain. Biasing voltage for this NMOS transistor is 0.55V and current is 867 µA.

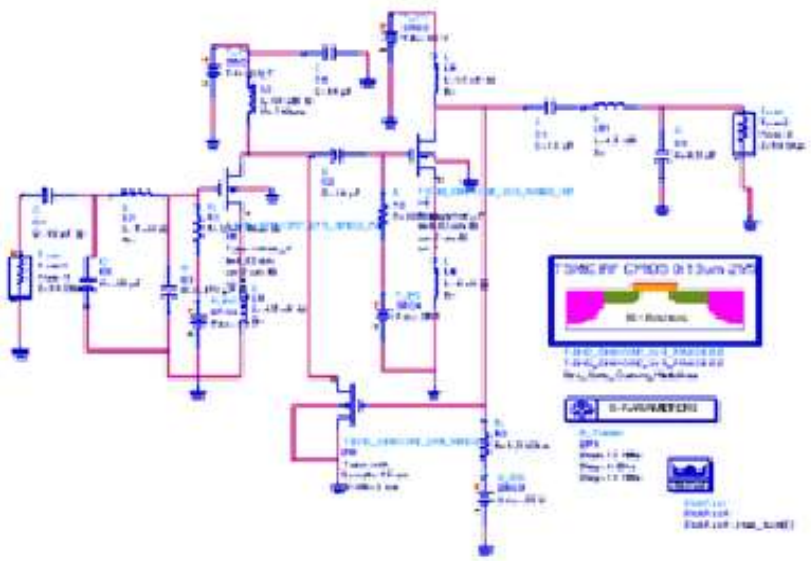

Figure 2. Schematic of an amplifier design

The above design, fig. 2 is implemented in the ADS. The S11 (input return loss), S12 (Isolation), S22 (output return loss) and S21 (gain) are plotted. The stability is checked of the overall circuit which is 1.5 i.e. above 1, and the noise figure is 2.1.

Positive Feedback Stage:
Positive feedback technique is used to achieve the high gain. Active device is used for the feedback. DC biasing is used to bias this active device.

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LAYOUT OF DESIGN:

With the LNA designed, the final step was the layout process. The layout process allows designers to have their circuits manufactured. Layout is an important step in RFIC design for several reasons. Layout determines the physical area that the LNA will occupy which is important as there are chip size specifications for wireless LAN transceivers. As well, the area the LNA should be minimized since the chip area for wireless LAN transceivers is limited.

More importantly, the physical layout of the LNA will have a direct impact on its performance. The performance is affected as the physical layout introduces parasitic, coupling. Layout was performed using the ADS layout tool.

The process that was used, CMOS 0.13µm, allows for 4 levels of metal to be used; the first level of metal is the most resistive while the top level of metal, the analog metal, is the least resistive. The metals are separated by a polysilicon layer. A connection between the metal layers is achieved using Vias. Vias provide a path from one metal to another, however they introduce resistance. To minimize the resistance, an array of Vias can be implemented.

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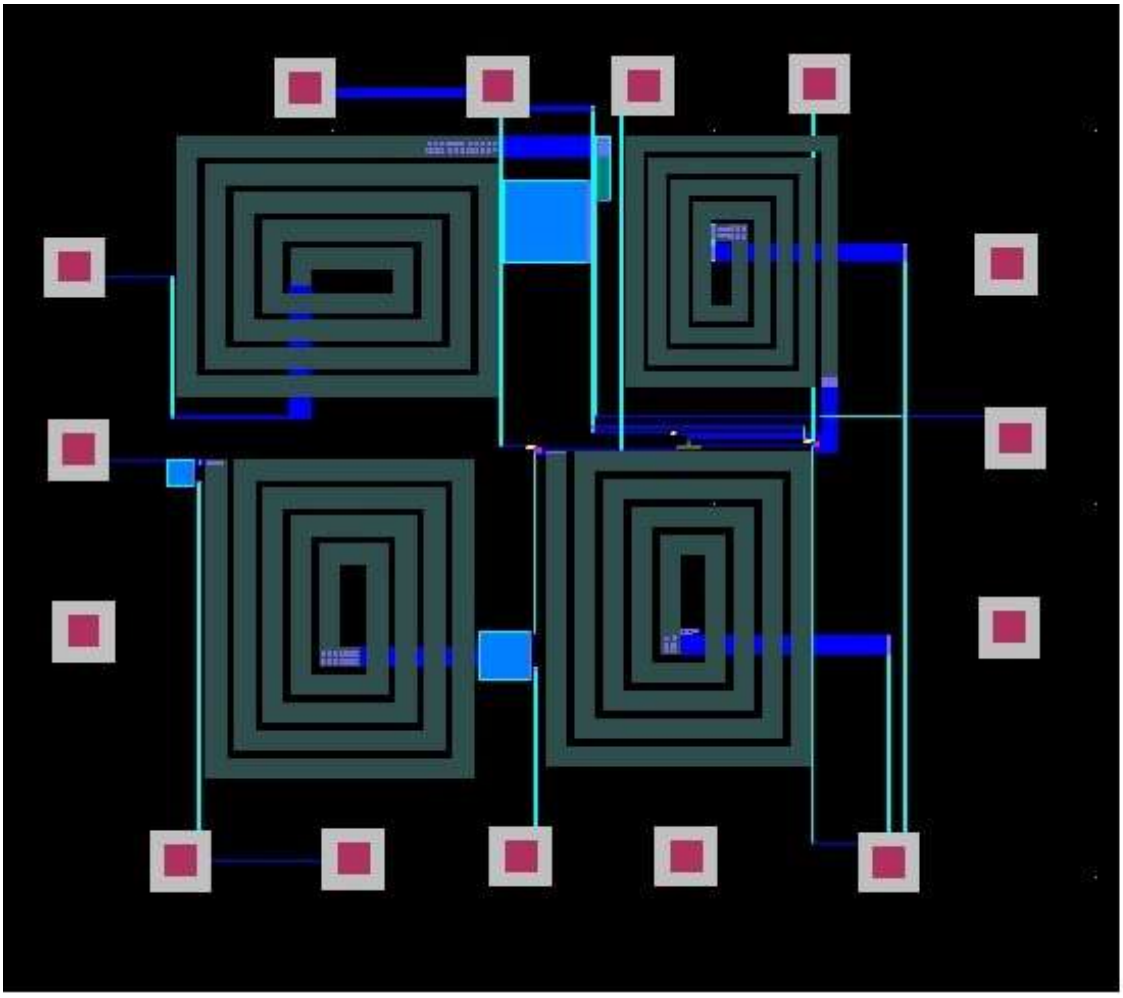

Figure 3. Layout of an amplifier design

Above figure 3 shows the layout of designed amplifier.

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RESULTS

ADS (Advance Design System) software is used for the simulation of the circuit. It is software developed by the Agilent Company. The parameters such as S11, S12, S21, S22, noise figure and stability are plotted for the designed circuit.

The noise related parameters are the noise factor (F) and the noise figure. The noise figure is defined as the difference between the SNR in and SNR out. Noise figure is required to be very less; in the implemented design the overall noise figure is 2.1dB.

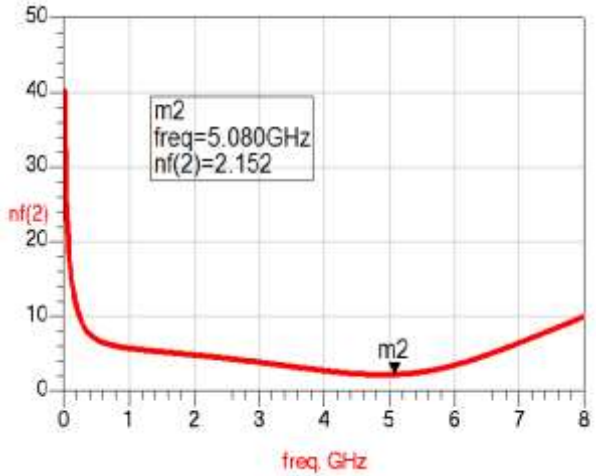

Figure 4. Noise Figure Vs frequency

Stability of the designed circuit is 1.5 which is greater than 1. It means the amplifier is having good stability and there are not any oscillations.

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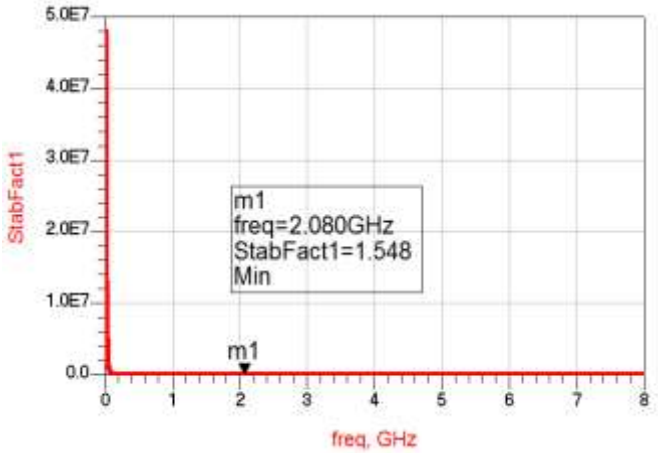

Figure 5. Stability Vs frequency

Input return loss (S11) is measured at the same port to calculate loss due to incident and the reflected signal. The ideal value of S11 should be below -10 dB. It shows signal reflected at port 1 for the incident signal at port 1. Similarly the S22 at the output port also should be below -10 dB.

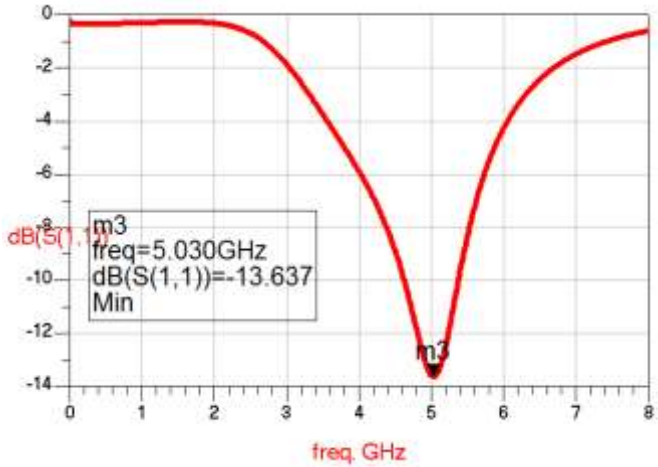

Figure 6. Input return loss Vs frequency

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Figure 6 shows the input return loss S (1, 1) measured at the input port 1. The S11 value is -13 dB at 5GHz.

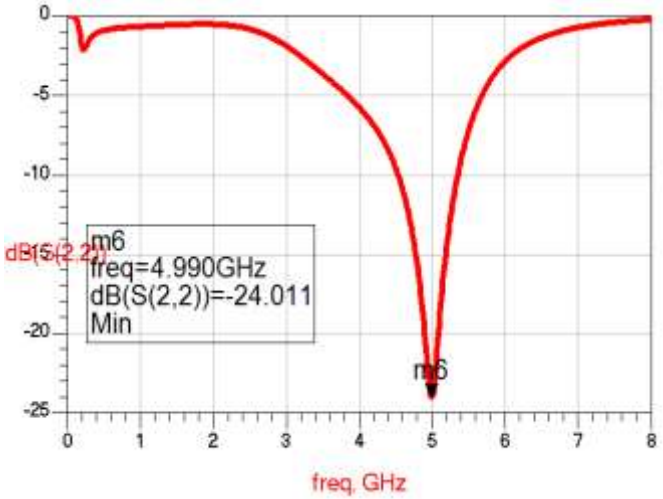

Figure 7. Output return loss Vs frequency

Figure 7 shows the output return loss S (2, 2) measured at the output port 2. The S22 value is -24 dB at 5GHz.

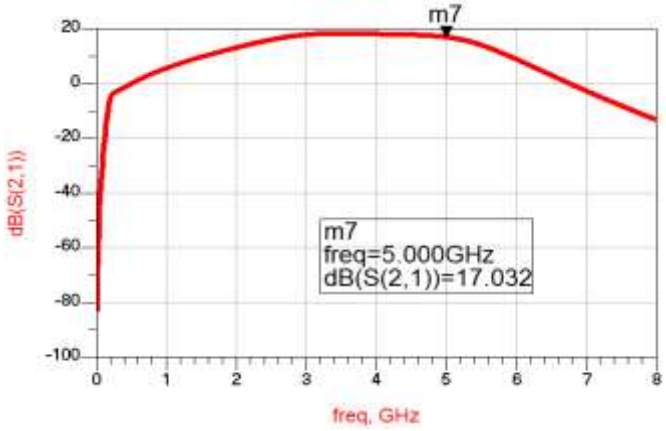

Figure 8. Gain Vs frequency

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Figure 8 shows the gain S (2, 1) of the overall circuit. Gain is 17 dB at 5 GHz.

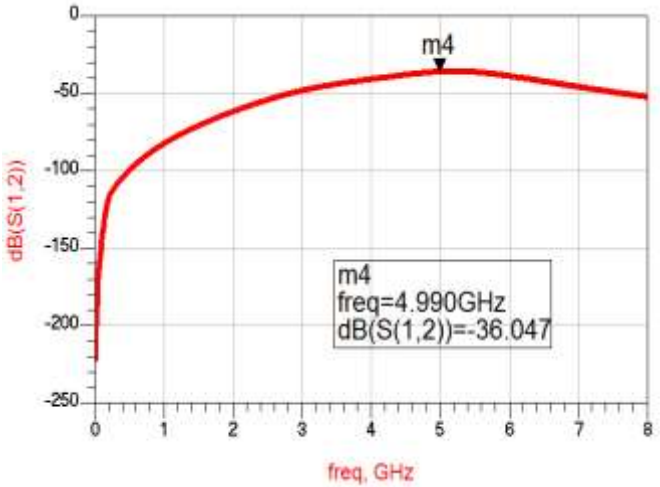

Figure 9. Isolation Vs frequency

Figure 9 shows the isolation S (1, 2) of the overall circuit which is -36 dB.

CONCLUSION

The amplifier is showing excellent gain, stability, noise figure, and input/output return loss. The simulation results show that the designed integrated circuit can meet the requirements of LNA. Complete LNA schematic is simulated in Agilent's ADS through 0.13µm CMOS technology generates 17 dB voltage gain (S21), 2.1 dB noise figure (NF), -10.078 dB input return loss (S11) and -13 and output return loss(S22) -24. Also, the stability factor is 1.548 at 5 GHz frequency with voltage supply of 0.6V.

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